New silicon based power devices will compete with SiC and GaN devices

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Silicon Power Devices

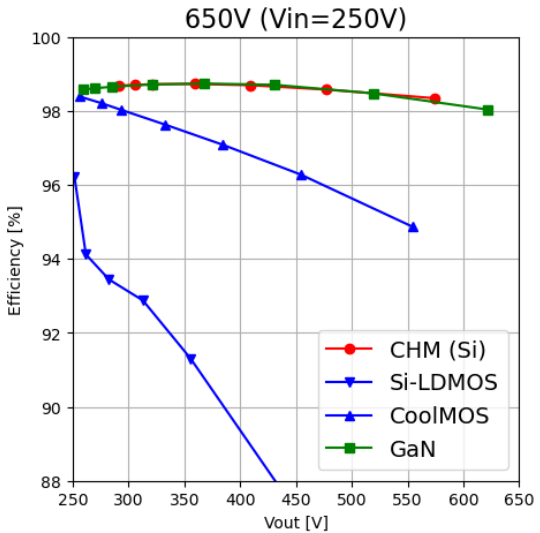
- A new LDMOS power device based on bulk Si, 60-1250V.
- Patented concept.
- Performance is about the same as for GaN and SiC based devices and much better than present state-of-the-art Si bulk devices
- Simulated product specifications and SPICE models at different voltages available.

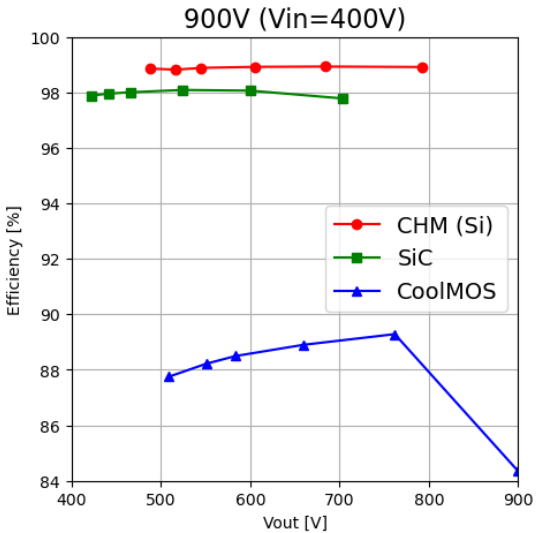
Performance Highlights

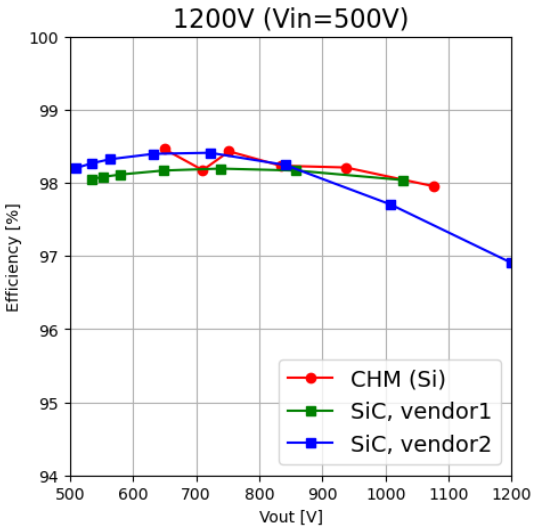
- Voltage range extended from 900V up to 1250V. The voltage range is now stated as 60-1250V.
- The die size is reduced by a factor 2 and this will more than double the number of good dies out from a wafer => die cost reduced by more than a factor 2.
- Output capacitance, C_{OUT}, has been reduced by around 30%, which will reduce switching losses.
- No external Schottky diode is required, which further reduce cost.

Comparison with GaN and SiC

- A Si LDMOS power device with efficiency about the same as comparable GaN and SiC devices at 650V, 900V and 1200V and being the first Si device to accomplish this.

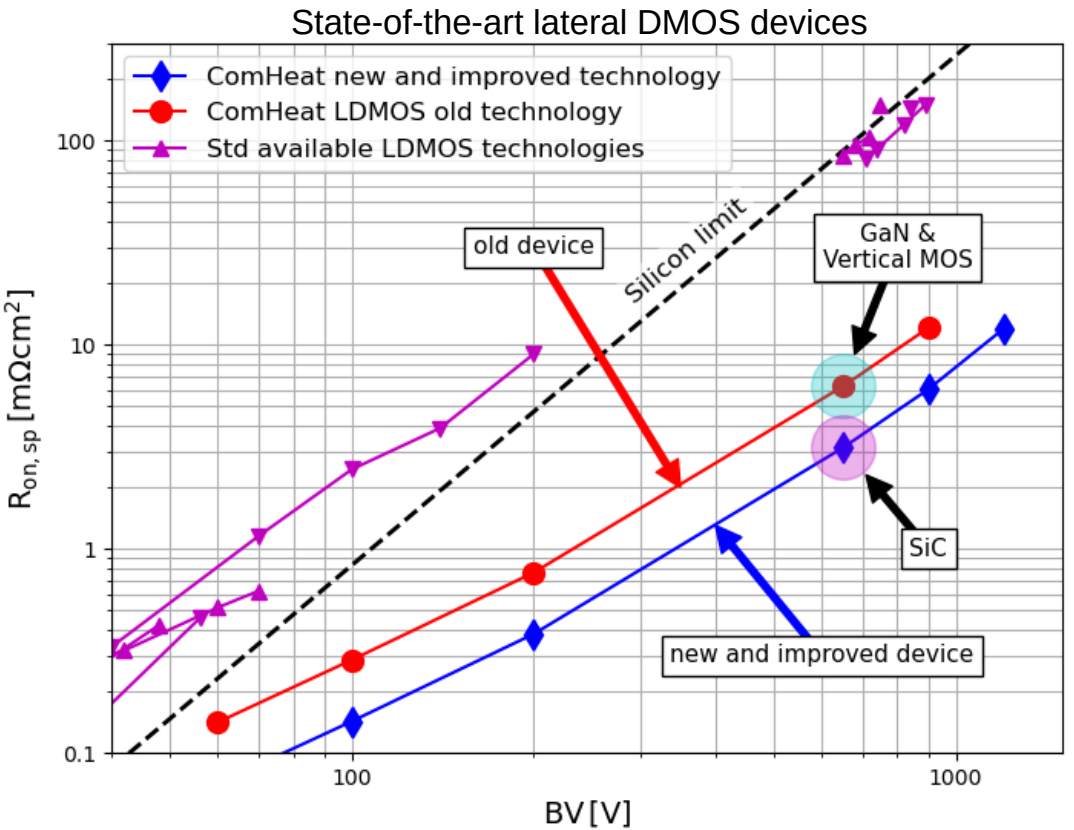






SPICE-simulation, Boost converter, 1 MHz

Ron*Area vs Breakdown Voltage



Reverse recovery comparison

- 100 mΩ, 650V device
- RR test conditions: 400V, 19A, 100 A/us

	ComHeat without external diode	CoolMOS with FD (external fast diode)	CoolMOS without FD
Qrr	1 uC	0.8 uC	9 uC
trr	50 ns	150 ns	470 ns

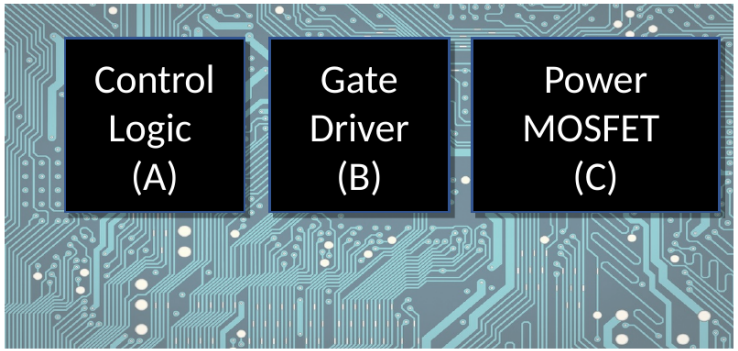
- From the comparison above it is obvious that ComHeat can get a similar low Qrr without a fast diode in parallel with the drain and body.
- This means lower cost and higher performance. An external diode adds area and capacitance.
- This concept is independent of voltage class.

Electrical data comparison – 650V

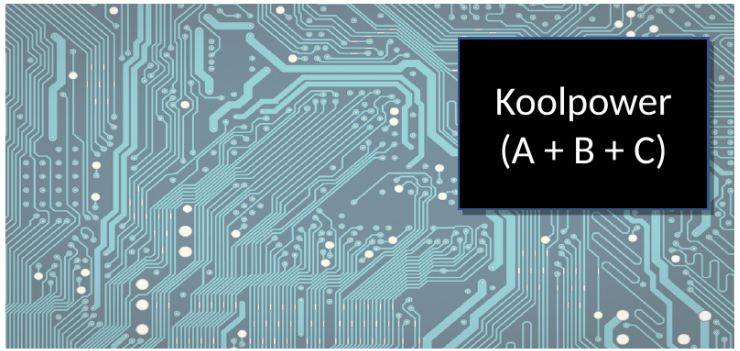
	ComHeat 650V (LDMOS)	Si SJ (vertical) IPZ65R095C7	SiC (vertical) C3M0060065D	GaN (lateral) GS66504B
$R_{DS,on}$	100mΩ	100mΩ	100mΩ	100mΩ
$V_{GS(Th)}$	0.5V	3.5V	2.3V	1.7V
C_{iss}	510pF	2000pF	600pF	120pF
C_{oss}	24pF	31pF	90pF	80pF
C_{rss}	0.01pF	2pF	9pF	0.8pF
Q_g	7nC	48nC	28nC	3nC

All devices normalized to 100mΩ, capacitances at V_G=0V, V_D=100V

Innovative LDMOS design on single die reduces size, achieves increased system integration and lower costs



3 devices into 1



Die reduction to 1/5th

Koolpower LDMOS

Status

- Ready to be implemented on Silicon.
- The implementation of the new power device will be based on standard available equipment and processes used in semiconductor industry.

Exercised opportunity

- We have had discussions with a Top 5 Fab House.
- They have seen process flow and device characteristics and concluded die sizes, performances, manufacturability were all in line with ComHeats expectations or better, and devices could be made very cost effectively.
- They would like to work with ComHeat and a "device" partner if a device partner would like to work with them for implementation.